IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 13, Issue 1 Ver. IV (Jan. – Feb. 2018), PP 82-90
www.iosrjournals.org

Low-Cost Test of An RF Mixer For Wi-Fi Applications

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Abstract: *This Paper Proposes A Variety Of On-Chip Monitors In Order To Implement A Low-Cost Test Methodology For Circuits And Radio-Frequency (Rf) Systems After The High Volume Production Stage. It Is Not The First Time That We Publish Such Monitors But The Aim Of Our Work Is To Extend The Library Of Rf Circuits Circuit Under Test (Rf Cut Lib) On Which Our Sensors Are Evaluated. Notice That For Each Rf Circuits The Proposed Monitors Must Be Adapted To Be Able To Present A High Test Coverage. The Monitors Are Called "Dummy Circuits" And "Process Monitors". These Monitors Have No Electrical Contact With The Circuit Under Test And Do Not Touch The Signal Path. In Fact, They Are Placed At The Layout Level Near The Circuit Under Test. Consequently, During The Manufacturing Process, They Follow Similar Process Variations As Those Of The Circuit Under Test. During The Test Step, The Performance Of The Rf Circuit Will Be Predicted From The Dc Measurements At The Output Of These Monitors Using The Alternative Test Technique. We Also Designed Other Monitors That Are Dc Probes, An Envelope Detector And A Current Sensor. These Monitors Are Physically Connected To The Various Critical Nodes Of The Circuit Under Test In Order To Detect Catastrophic Faults That May Occur In The Circuit Due To An Imperfection In The Manufacturing Process. The Introduction Of These Monitors Degrades The Performance Of The Circuit Under Test Which Requires A Co-Design Effort To Meet The Pre-Defined Specifications. The Proposed Monitors Will Be Now Evaluated Using Post-Layout Simulations On A Rf 2.4 Ghz Mixer Used For Wifi Applications.*

Keywords: *Built-in Test, RF Test, machine learning, RF design*

Date of Submission: 16-02-2018 Date of acceptance: 03-03-2018

I. Introduction

Nowadays, SoCs (System on Chip) are composed of digital (eg DSP: Digital Processing Unit), analog and mixed blocks (e.g. analog and digital-to-digital converters) and RF circuits (e.g. amplifiers, mixers, filters). These chips are used in different applications such as biomedical equipment, mobile phones, Wi fi communications, Bluetooth etc. This recent explosion of the single-chip integrated systems market has put analog and radio frequency circuits at the forefront. In fact, once the design of these circuits is validated, they are sent to large volume production to make thousands of samples. During the manufacturing step in clean rooms, catastrophic faults can occur (e.g. a short circuit between two parallel metal lines or between the two terminals of a component, an open circuit that cuts the metal line connecting two components etc.). Other types of defects are parametric defects. They derive from a wide variation in the manufacturing process which implies a wide variation in the process parameters and in the electrical parameters of the circuit (e.g. variation of the channel length of a transistor, variation of the thickness of the gate oxide, variation of the threshold voltage). These types of faults make the circuit defective, hence there is a need for a step that follows the manufacturing of any IC. This step consists in testing all the circuits manufactured in order to validate their functionality as well as their predefined performances to verify id they respect the specifications; this is called the production test. Currently, the testing of analog / RF circuits is underdeveloped because of the complexity of analyzing analog signals. In other words, the difference between a valid or bad response is, in general, clearly defined for a digital circuit (0 or 1). On the contrary, for an analog / RF circuit having at its output a variable continuous signal as a function of time, it is difficult to judge whether the circuit is in the margins of the specifications or not. This reality directly influences the cost of testing analog / mixed / RF circuits which is currently 80% of the test cost, noting that the surface of these circuits represents only 30% of the total area. This test cost mainly depends on equipment costs as well as their maintenance and testing time which is strongly related to the time to market [1]. As a result, our research consists of presenting a low-cost test methodology for RF circuits.

The industrial test of the RF circuits consists to adopt an approach that aims to measure sequentially all the performances of each circuit. The test of each performance requires: a) a special configuration of the circuit under test with the hardware dedicated to test this performance; b) the application of a test stimulus which is a specific signal, dependent on the measured performance, to be applied to the circuit under test. It can therefore be deduced that the measurement of the performance of each circuit requires passing through different configurations, recalling that this approach must be carried out for all the circuits manufactured. This entire

procedure explains why the test time of mixed / RF circuits accounts for 60% of the total test time of a chip. In addition, this time depends on the number of chips to be tested, their complexity, the capacity and speed of the equipment and the number of performances to be validated. This procedure also requires fairly complex and expensive automatic test equipment (ATE: Automatic Test Equipment), especially those dedicated to the testing of RF circuits. Several techniques have been proposed to reduce the cost and the test time including the off-chip test, the on-chip test and the alternative test.

The off-chip test aims to migrate the main functions of the test equipment to a load board in order to use less expensive testers [2]. For example, designing a PCB with a stimulus generator, analog-to-digital and digital-to-analog converters, modulators and demodulators as well as multiplexers. The in-house development of these PCBs is a great challenge at the design level especially with respect to the specific constraints to be taken into account in the case of RF circuits. The on-chip test consists of designing a tester on the chip [3], reconfiguring the circuit under test to increase its testability [4] and finally an intelligent solution which consists of designing simple circuits (on-board monitors) providing their outputs with low-frequency or DC signals that follow the performance of the circuit under test [5], [6], [7], etc.

During the on-chip test, the outputs of these monitors are measured to judge whether the circuit under test is good or bad based on pre-defined limits. Finally, a last proposed technique is the alternative test which consists in predicting the performances of the circuit starting from the low frequency or DC measurements by using techniques of statistical regression [8], [9], [10]. The purpose of predicting performance is not to discard all circuits that do not meet certain predefined specifications, but rather to consider their use in other applications.In this paper, we follow the on-chip test methodology combined with the alternative test. A variety of monitors that monitor an RF front end and have DC outputs correlated with front-end performance are being studied. We propose "fictif/Dummy" circuit and process monitors placed near the circuit under test and which do not touch the main path of the RF signal but follow the same process variations; they will be able to detect large parametric variations that can damage the circuit. Therefore, the output measurements of the on-chip monitors are correlated to front-end performance (eg S-parameters, NF, IIP1, IIP3) using the alternative test approach.In addition, the study on the RF mixer concerns other monitors existing in the literature and developed with simpler architectures such as DC probes, an envelope detector and a current sensor. These monitors are physically connected to the different critical nodes of the front end, so they are able to detect catastrophic faults that may occur in the circuit.

The rest of the paper is structured as follows. In the next section, we discuss in more detail the advantages of the on-chip test combined with the alternative test while presenting the challenges faced. New monitors are presented in section III. Monitors physically connected to the circuit under test, are presented in section IV. The case study is presented in section V. The experimental results are presented in section VI. Section VII concludes this work and presents perspectives for future work.

II. On-Chip Test Technique Combined With Alternative Test

Nowadays, one of the best solutions proposed to solve conventional test problems, in terms of cost and time, is the alternative test. [8], [9], [10] show that the variation of the process parameters of a circuit (e.g. the length or width of a transistor, the value of a resistance or capacitance) affects its performance (ex. gain, noise figure etc.). Also, these variations affect the measurements that can be extracted from this circuit (e.g. the samples of the response of the circuit under test to a stimulus). As a result, for a statistically significant sample of circuits, a function linking performance to measurements can be constructed using regression tools. Once this function is built, any performance of the circuit under test can be predicted from the DC measurements. It is important to note that the performance and measurements necessary to build the regeneration function must derive from a population of chips representative of process variations. In our study, the approach we adopt is to combine the alternative test with the on-chip test by considering as measurements the output signals of the on-chip monitors. The big challenge is to design simple architectures for such monitors with outputs that follow the behavior of the circuit under test. Other challenges that may be faced are: 1) Ideally, the monitor should not degrade the performance of the circuit under test; however, it is necessary to co-design them together in order to respect the predefined performances of the circuit under test, 2) The evaluation of these monitors is necessary in order to check if a fault in the circuit under test is not detected by the monitors and therefore it passes the test (bad acceptance), and conversely a functional circuit will be rejected (bad rejection) [11].

However, this approach greatly reduces the cost of the test for two reasons: a) low frequency outputs or DC monitors are measured with a low cost tester, b) based on the alternative test approach, these outputs may be able to predict the performances of the circuit under test from a single configuration and a single test stimulus, which greatly reduces the test time.

III. New On-Chip Monitors: "Fictif" / Dummy Circuits And Process Monitors

3.1 Basic idea

The different steps in the manufacturing process induce variations in process parameters that affect components and interconnections. This results in two categories of variation: inter-die variations and intra-die variations: The inter-die variations include the lot-to-lot, wafer-to-wafer and die-to-die variations. They are defined as being the average variations of a process parameter in the same way for all structures in a single chip.

Lot-to-lot variation is a variation of the average of a process parameter from one manufacturing batch to another. Wafer-to-wafer variation is a variation of the average of a process parameter from one wafer to another in the same production batch. Die-to-die variation is the variation of the average of a process parameter from one chip to another in the same wafer.

Intra-die or mismatch variations include the variation of the average of a process parameter from one structure to another in the same chip, for example the variation of the length of the channel calculated on different circuits in the same chip. Therefore, any two structures embedded in the same chip are affected in the same way because of inter-die variations. In our case, the "fictif/dummy" circuits or process monitors will be placed near the RF Mixer. We can therefore assume that, for a specific design of these monitors, the performance of the circuit under test and the output measurements of the circuits and process monitors are strongly correlated, since they are impacted by the same inter-die variations.

On the other hand, the intra-die variations affect differently the circuit under test and the offered monitors. For mature technologies (> 65nm), variations related to the inter-die component are the forms of the variations most often considered. Variations related to the intra-die component are smaller but still exist. For less mature technologies, intra-die variations are moderate by performing layout precautions and using the regression function (averaging a random quantity). Based on this observation, we proposed to place at the layout level the "fictive/dummy" circuits and the process monitors to be able to monitor the RF front end virtually while predicting its performance without affecting the signal path and therefore without degrading it.

3.2 "Fictif" / Dummy Circuits

The circuits are very simple circuits as shown in FIG. 1. They mimic common structures already present in the circuit under test (FIG. 4) and allow the extraction of the behavioral parameters (e.g. the gain of a MOS stage, the gain of a current mirror) whose variations are defined indirectly by process parameters. In this study, two types of fault circuits are tested: a polarization circuit with a current mirror and two MOS transistor amplifiers with different geometries. These circuits are biased by DC voltages generated on-chip and provide their outputs DC signals. They occupy a small area and they do not degrade the performance of the circuit under test. However, it is recommended that the transistors have similar geometries to the existing transistors in the circuit under test because the process variations also depend on the geometry of the component.

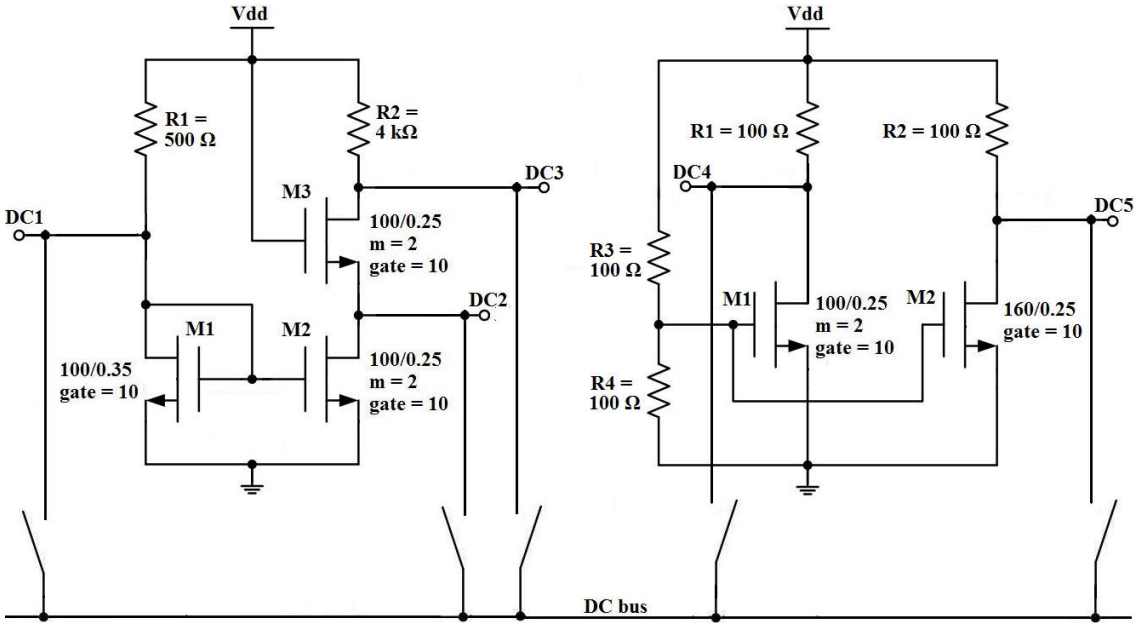

Fig. 1. Fictif/Dummy circuits: (a) polarization circuit with a current mirror and (b) Gain stages with different geometries.

3.2 Process-Monitors

Process monitors are basic components that directly measure a process parameter (e.g. the value of a capacitance per unit area or the reverse current of a bipolar transistor). It is clear that the variation of the value of a capacity during manufacturing is directly related to process variations. In this work, we use a MIM capacitors that mimics the geometry and layout of the existing capacitors within the Mixer. Therefore, any variation in these capacitors can be followed by the MIM capacitors.

IV. Monitors on-Chip Physically Connected To The Circuit Under Test

In the previous section, we have seen the interest of the dummy circuits and process monitors since they virtually test the circuit under test without any electrical contact. However, these circuits can never detect a random catastrophic fault that can exist in the front-end. This problem has no other solution for the moment than the use of monitors electrically connected to the circuit under test.

4.1. DC PROBES

The simplest way is to connect DC probes to the different critical nodes of the circuit to be able to detect the majority of the defects. A DC probe consists of a large resistance to avoid as much as possible degradation of the performance of the circuit under test. The disadvantage of DC probes is that they cannot detect a short-circuit at the inductance level or an open circuit at the capacitance level.

4.2. ENVELOPE DETECTOR

We have designed an envelope detector, having a simple architecture, shown in FIG. 2. It comprises a rectifier followed by a low-pass filter. The rectifier consists of Ipol, M1 and M2 which is polarized in low inversion. The operating point is controlled by the bias current which passes through the diode-connected transistor M1. The potential difference between the gate and the M2 source is at the limit of the conduction point. When the current passing through C1 is positive, the transistor M2 is turned off and the current passes through the transistor P1 to ground. During the negative alternation of the current, the voltage at the source of M2 decreases which makes it go. The current is thus redressed and will then be copied and amplified through the current mirror formed by the transistors P2 and P3. The second stage is a low-pass filter in which the trade-off between the settling time constant and the output voltage ripples must be taken into account.

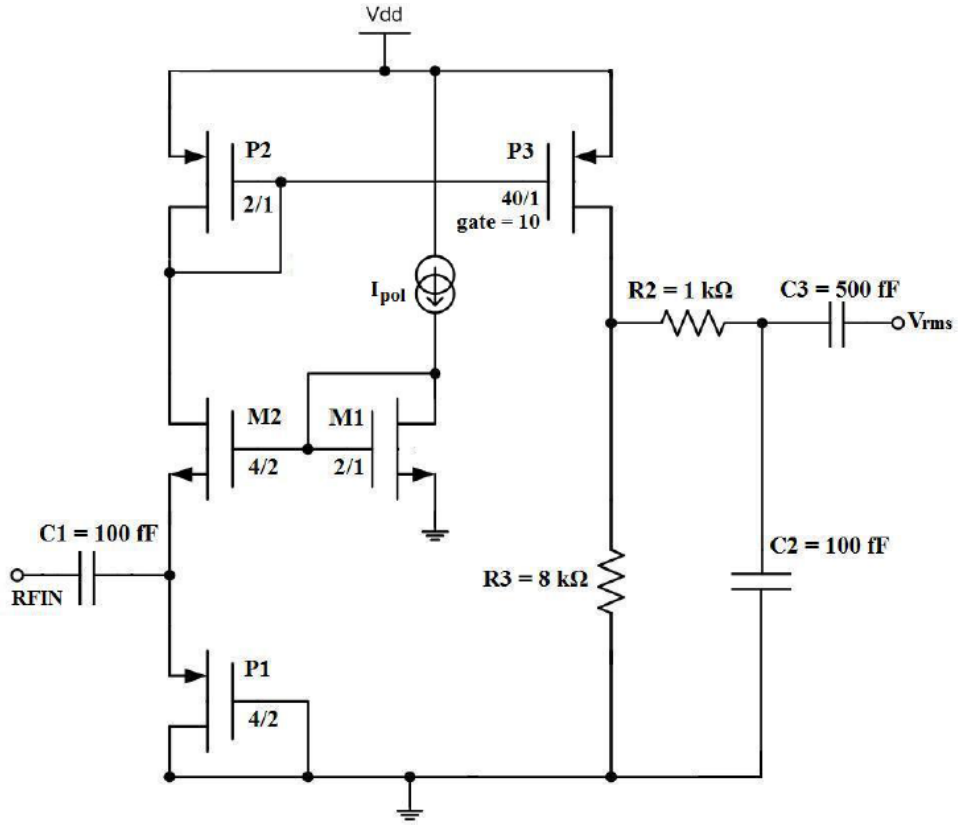

Fig. 2. CMOS Envelope Detector

4.3. CURRENT SENSOR

A current sensor is provided for extracting the information corresponding to the power supply current. We adapt the current sensor proposed originally in [12] to our design and technology. This sensor uses the resistance ρ of the line that connects the circuit under test to the supply voltage. This resistance of a few ohms makes it possible to follow the variation of the supply current by a voltage drop across the resistor which unbalances the PMOS current mirror formed by P1 and P2, which results in an RF current at the output of the sensor. proportional to the dynamic current of the circuit under test. In order to obtain the RMS value of the Imeas current at low frequency, the output of the current sensor is connected to the input of the envelope detector.

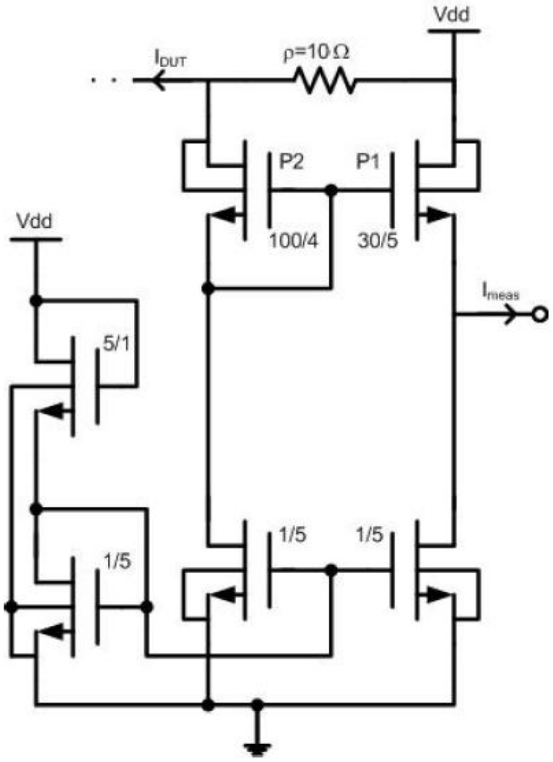

Fig. 3. CMOS Current Sensor

V. Case Study

Our case study is an RF mixer for WiFi applications. The mixer is a Gilbert cell mixer needed to transpose the signals from high-frequency to low-frequency signals. Figure 4 illustrates the RF Mixer with the various on-chip monitors (the fictive circuits and process monitors are not shown). In order to minimize the number of pins, an analog DC bus combined with switches is designed from a decoder and a simple register. So in total two pins will be added to the chip, one input to select one of the monitors and one output to recover the different DC measurements.

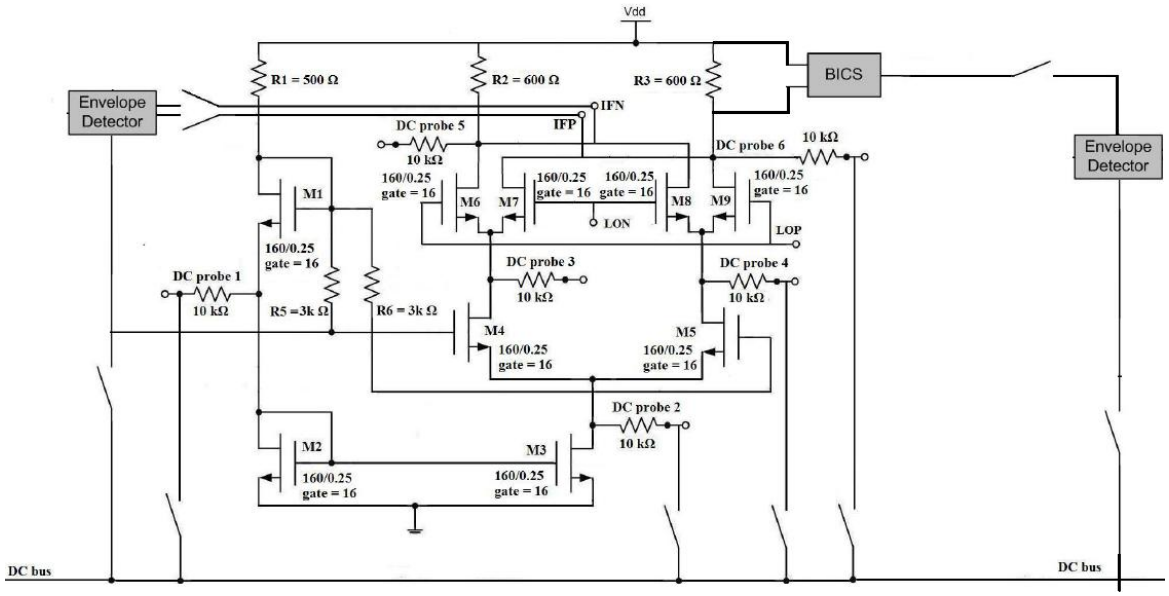

Fig. 4. The electrical scheme of the RF Mixer with on-board monitors.

VI. Experimental Results

Figure 5 shows the RF front-end layout and the different monitors designed with NXP semiconductor's Qubic 4 plus 0.25 µm technology. A particular interest is to take into account the capacitances, resistances, inductances as well as parasitic mutual inductances. The noise extraction is performed using the Assura tool under Cadence and the circuits are resized to meet the performance of the RF front-end. The following analysis is based on post-layout simulations performed by Spectrum RF at a rate. Tables I shows the performances of the Mixer when they are alone without the on-chip monitors and shows the performances degradation following the insertion of each of the monitors. It can be observed that the current sensor seriously degrades several performances, however the other monitors are less intrusive. The last column shows performance after final co-design.

The envelope detector has the following characteristics: 1.5-11KΩ in a frequency band of 500MHz - 10GHz and an input dynamic of 35dB as shown in figure 6. Similarly, the current sensor has an operating frequency of 100MHz-10GHz and an input dynamic of 30 dB as shown in figure 7.

The Mixer occupies a surface area of 6800 um², respectively. The envelope detector and the current sensor occupy 1820 µm² and 2800 µm², respectively, while the area of the fault circuits, the MIM capacitance and the DC probes is too much smaller i.e. negligible.

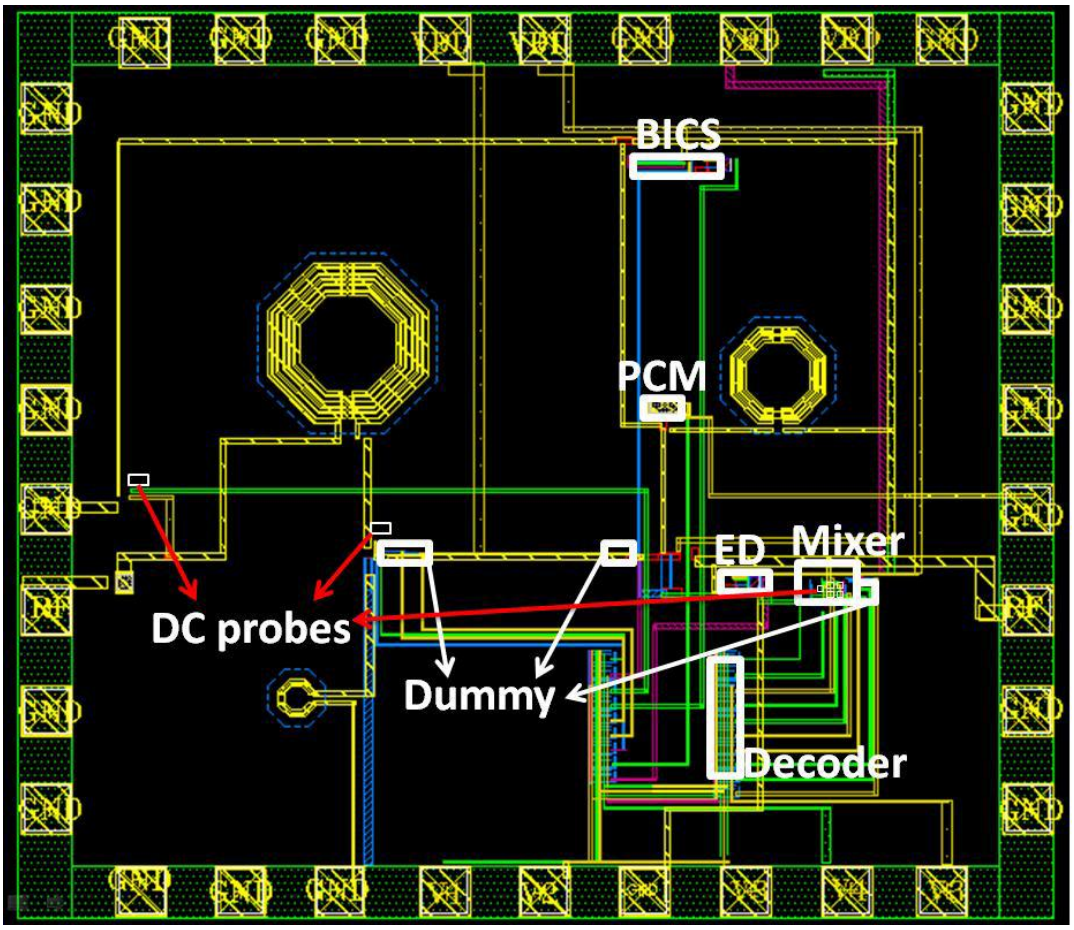

Fig. 5. Layout of the Chip

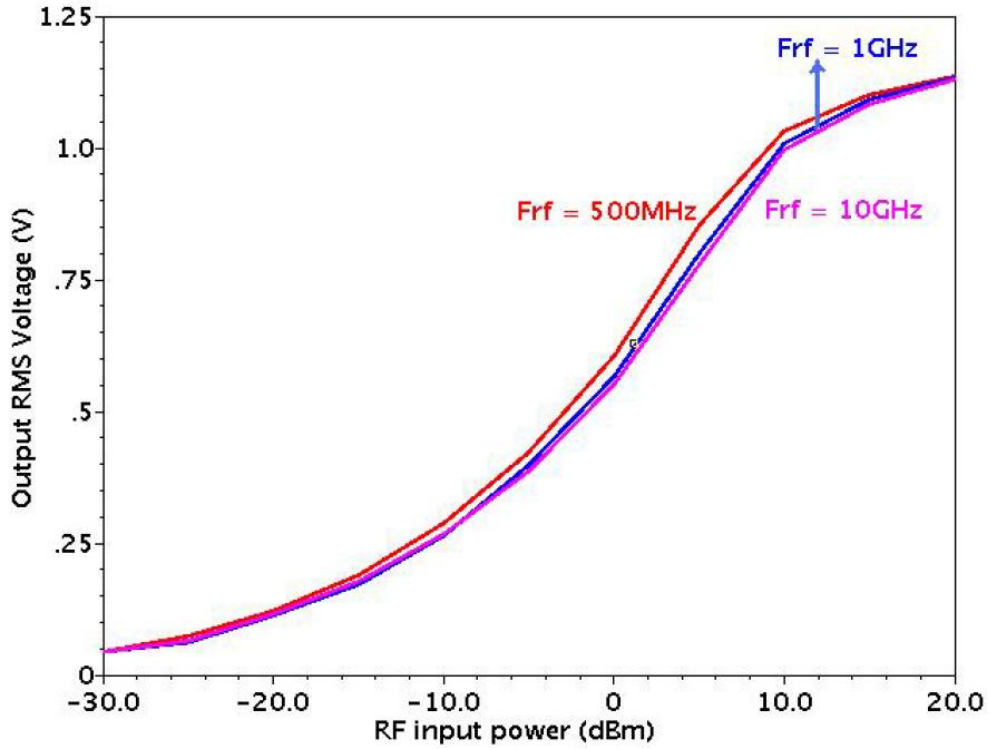

Fig. 6. Characterization of the envelope detector.

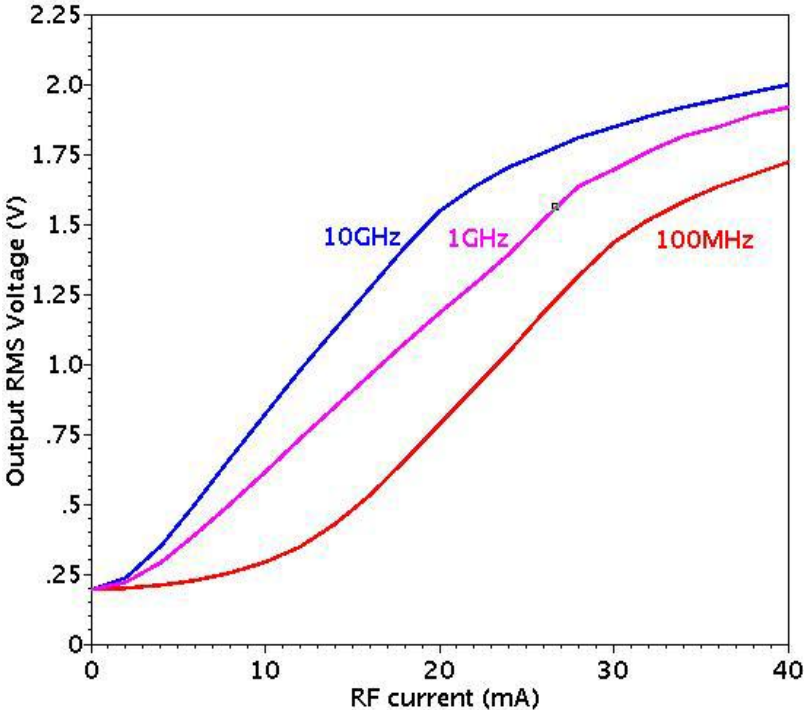

Fig. 7. Characterization of the current sensor.

Table I: Performances Of The Mixer

	Only Mixer	With DC probes	With Envelope Detector	Final Co-Design
Gain (en dB)	14.29	12.51	13.71	14.17
NF (en dB)	14.067	14.2	13.97	14.048
1-dB CP (en dBm)	-12.27	-13.1	-13.38	-12.68
IIP_3 (en dBm)	-2.7	-3.22	-2.22	-2.4

Figures 6 and 7 show the input-output characteristics of the envelope detector and the current sensor for the operating frequency limits.

Monte-Carlo post-layout simulations are performed to obtain 1000 front-end instances. Among these 1000 instances, 700 are used to train the regression function between the performance and the output measurements of the on-board monitors and 300 instances to validate its accuracy.

Table III shows the prediction errors of the RF Mixer performances by considering a combination of different measurements. It can be seen that the proposed fictive circuits circuits and process monitors are able to predict the performance of the RF Mixers.

Table Iii - Rms Errors Of Predictions (In%) Of The Rf Mixer Using Different Combinations Of On-Road Monitors

	Gain	NF	1-dB CP	IIP_3
All Sensors	0.56	0.4	0.21	1.7
Fictive/Dummy Circuits Process Monitors	0.91	0.65	0.21	2.02
Fictive/Dummy Circuits Process Monitors Envelope Detectors DC probes	0.71	0.68	0.21	1.91

VII. Catastrophic Fauls Analysis

In order to study the rate of detection of catastrophic faults, 52 were injected within the Mixer at the layout level, including all possible short circuits and open circuits.

A short circuit is modeled by a metallic connection that connects the two extremities of a component while a circuit Open is modeled by the cutting of the metal line.

After the injection of each fault, the parasites are extracted and the extracted view simulated to check whether the on-chip monitors physically connected to the RF Mixer detect faults or not. The result of the analysis shows that, for this model of the injected faults, the DC probes 1 and 2 in the Mixer and an envelope detector connected to the RF Mixer output are sufficient to detect all the defects. These monitors added to the fictive circuits and to the process monitors will be chosen to test such a case study.

VIII. Conclusion

In this paper, we studied a variety of embedded monitors for testing an RF mixer dedicated to WiFI applications. Fictive circuits and process monitors are able to predict RF front-end performance without affecting the signal path. In addition, two DC probes connected to the polarization stages of the Mixer and an envelope detector connected to the mixer output are required to detect the most likely catastrophic faults during the manufacturing. Future work aims to select new monitors that do not touch the path of the RF siganl and that can detect catastrophic faults in a circuit.

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IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) is UGC approved Journal with Sl. No. 4198, Journal no. 45125.

Louay Abdallah. " Low-Cost Test of An RF Mixer For Wi-Fi Applications." IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) 13.1 (2018): 82-90.